REMARKS

CLAIM REJECTIONS – 35 U.S.C. § 102

Claim 1 has been rejected under 35 U.S.C. § 102(e) as being anticipated by Dimenstein, U.S. Patent No. 6,732,275. In order for there to be anticipation, each and every one of the claims must be found in a single reference. It is respectfully submitted that the claims, as amended, recite subject matter clearly not disclosed or suggested by the Dimenstein patent. In particular, the claims, as amended, recite that the peripheral includes a timing generator, as well as a digital-to-analog controller for controlling the timing of the decoded/decrypted data to the digital-to-analog controller for playback by an external analog device. No such structure is disclosed or suggested by the Dimenstein patent. In fact, the Dimenstein patent teaches playback of the digital data on the PC itself. The Dimenstein patent also teaches that "(c)ontrol and timing signals are applied from PC 110 to microprocessor base digital signal processor 214 of device 120, and its internal memory 216 (Dimenstein, Col. 5, lines 46-48). In addition, the Dimenstein patent teaches that the decryption code is generated by the PC and passed to the peripheral device by the PC (Dimenstein, Col. 4, lines 61-63). The claims recite a totally different system in which the decryption code and timing signals are resident within the peripheral, thus minimizing the control and decryption signals that must be sent from the PC to the peripheral. For these reasons and all of the above reasons, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Appl. No.: 09/833,173
Amdt. dated: 4/12/2005
Reply to Office Action of October 12, 2004

Respectfully submitted,

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